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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,327	09/28/2001	Alaa F. Alani	A2-4059 1496.00150	3179
7590	11/15/2005		EXAMINER	
LSI LOGIC CORPORATION 1551 MCCARTHY BLVD., MS: D-106 PATENT LAW DEPARTMENT MILPITAS, CA 95035			DUNCAN, MARC M	
			ART UNIT	PAPER NUMBER
			2113	
DATE MAILED: 11/15/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/966,327	ALANI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Marc Duncan	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 20 October 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-3 and 5-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-3,5,7,8,10-14,18 and 19 is/are rejected.
- 7) Claim(s) 6,9 and 15-17 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 20 December 2004 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____                                    |

**FINAL REJECTION**

***Status of the Claims***

Claims 10-14 and 18-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Song et al. (2345423 A).

Claims 1-3, 5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al. (2345423 A) in view Microsoft.

Claims 6, 9 and 15-17 are objected to.

***Allowable Subject Matter***

The indicated allowability of claims 4 and 20 is withdrawn in view of the newly discovered reference(s) to Song et al. Rejections based on the newly cited reference(s) follow.

Claims 6, 9 and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10-14 and 18-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Song et al. (2345423 A).

Regarding claim 10:

Song teaches:

- (A) monitoring signals for transitions using a plurality of transition signals on a plurality of independent lines, each of said transition signals indicating a transition direction of one of said signals (page 4 lines 12-14 and page 10 lines 1-12);
- (B) inverting said signals only in response to at least a predetermined number of said signals transitioning to a particular logic state (page 10 lines 1-12);
- (C) presenting said signals on a transmission bus (Fig. 3 – 42).

Regarding claim 11:

Song teaches wherein said particular logic state is one of a (i) high logic state and (ii) a low logic state in Fig. 4. High and low are the only available logic states.

Regarding claim 12:

Song teaches wherein said predetermined number is greater than one half of a total number of said signals on page 13 lines 2-4.

Regarding claim 13:

Song teaches generating a plurality of transition signals each indicating a transition direction of one of said signals on page 10 lines 1-12.

Song teaches generating a flag signal when at least said predetermined number of said transition signals indicate said transition direction is to said particular logic state on page 10 lines 1-12 and in Fig. 5 – REV.

Regarding claim 14:

Song teaches the step of presenting said flag signal on said transmission bus in Fig. 3 – REV.

Regarding claim 18:

The claim is rejected as the means for performing the method of claim 10.

Regarding claim 19:

Song teaches wherein said predetermined direction is one of (i) a high to low direction and (ii) a low to high direction on page 10 lines 1-12 and page 11 lines 11-13.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al. (2345423 A) in view Microsoft.

Regarding claim 1:

Song teaches a circuit configured to:

(i) monitor a plurality of signals for transitions (page 4 lines 12-14) and

(ii) invert said signals when at least a predetermined number of said signals transition to a predetermined logic state (page 10 lines 1-12); and

wherein said circuit comprises:

(i) a transition checker circuit directly receiving said signals (Fig. 3 and 5) and configured to present a plurality of transition signals each indicating a transition direction of one of said signals (Fig. 5 – TS1-18)

(ii) a control circuit configured to present a flag signal when at least said predetermined number of said transition signals have said predetermined direction (Fig. 5 – 50) and

(iii) an inverter circuit configured to invert said signals in response to said flag signal (Fig. 7 – INV1-18).

Song does not explicitly teach a plurality of buffers configured to present said signals received from said circuit on a transmission bus. Song does, however, teach transferring a plurality of digital signals between two different devices on a plurality of lines.

Microsoft teaches a plurality of buffers configured to present said signals received from said circuit on a transmission bus in the definition of buffer (page 66).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the buffers of Microsoft with the data transmission circuit of Song.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because buffers allow timing corrections to be made to a data stream and allow devices of different rates to be connected to each other.

Regarding claim 2:

Song teaches wherein said particular logic state is one of a (i) high logic state and (ii) a low logic state in Fig. 4. High and low are the only available logic states.

Regarding claim 3:

Song teaches wherein said predetermined number is greater than one half of a total number of said signals on page 13 lines 2-4.

Regarding claim 5:

The combination teaches wherein said buffers are further configured to present said flag signal on said transmission bus in Song, Fig. 3. Song clearly teaches to send the flag signal on the transmission bus, and the combination necessitates data on the transmission bus to be sent through the buffers, hence the flag signal would necessarily be presented by the buffers.

Regarding claim 7:

Song teaches wherein said circuit further comprises a plurality of first flip-flops configured to store said signals as presented by said inverter circuit in Fig. 7 – CSW1-18.

Regarding claim 8:

Song teaches wherein said circuit further comprises a clock configured to present a clock signal to said first flip-flops in Fig. 3 – DCLK.

### ***Conclusion***

Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 10/20/05 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc Duncan whose telephone number is 571-272-3646. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md

  
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